Quantum Power Synchronous Multiplexer

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# Points to discuss

1. Value of the input impedance of the multimeter to be used. In principle there are two options: i) Agilent 3458 (Zin~10 GΩ//240 pF); ii) NI-5922 (Zin~1 MΩ//60 pF). The uncertainty due to the series resistance depends on the multimeter input resistance and the measurement configuration. In case of “absolute measurement configuration”, e.g. the digitizer is measuring Chx directly, the error is determined as a voltage divider:

Error = RON / (RON + ZV).

Then, a maximum value to the on-resistance must be established. Nevertheless, in case of differential sampling technique, such as using a quantum voltmeter, the influence of the series resistance could be neglected. The on-resistance could be reduced by connecting in parallel spare switches of the same IC.

1. ON and OFF-time. Fast commuting time (100 ns) can be obtained with an analog switch (ADG1411 or similar). Instead, photovoltaic relays have lower on-resistance and larger ON-time (3 ms).
2. Maximum input voltage, 10 V peak (7 V RMS). If input voltage lower than 5 V is accepted, it is possible to use analog switches with lower series resistance.
3. The power supply for the switching board is isolated from the main supply.

# Introduction

The aim of this document is to establish the requirements and description of the quantum power synchronous multiplexer (QPM).

## Requirements

Flexible design to multiplex between different voltage signals with the following characteristics:

1. Channel requirements
   1. Maximum input voltage: 10 V peak
   2. Maximum signal frequency: 1 kHz
   3. Turn on/off time: 1 μs
   4. Differential signal
   5. Coaxial design
   6. Bounce-free operation
   7. Uncertainty contribution < 0.1 ppm
2. Functional requirements
   1. Switching synchronized with an external signal
   2. Flexible design
   3. Two modes of operation are required by users:
      1. chopper mode: the digitizer takes one sample, or a small number of samples, of each channel within a signal period.
      2. alternating mode: the digitizer takes a fixed number of periods of each channel.

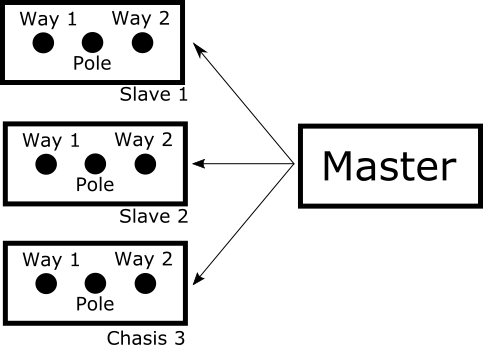
## Working Conditions

* The sources are considered grounded and with negligible output impedance.
* The measured signals are considered differential.
* The meter is considered floating and with a guard connection. In principle, the multimeter HP3458 will be used.

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# Multiplexer description

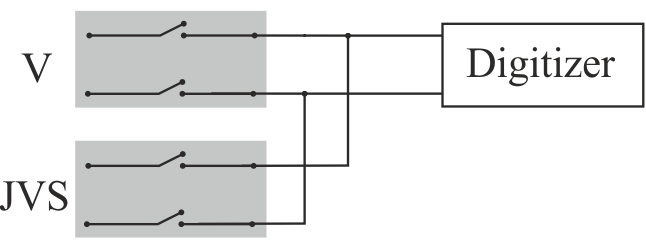
The multiplexer will be built in a modular form, with a master board that will control slave boards and will include timing functionalities. The slave boards will have a single pole and double throw. The user can use many of them controlled by the master, as the next figure shows.



**Figure 1:** three slave boards controlled by a single master board.

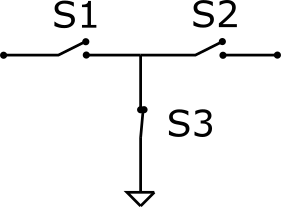
## Slave board

The slave board will include two throws and one pole, as the next figure shows. The signals are considered differential, so the switch commutes positive and negative terminals of the voltage source. The slave board must be reversible; it can be considered as 2 inputs - 1 output (2-to-1) or 1 input - 2 output (1-to-2).



**Figure 2:** slave board diagram.

Each switch will be arranged in T configuration using three solid-state relays in order to improve the overall off-isolation. S1 is connected to the voltage source and its output is connected with two relays. S3 connects the signal path to ground and S2 connects the signal path to the output of the board. See the next figure.



**Figure 3:** the switches are connected in T configuration.

To reduce the series on-resistance of the T configuration the spare switches in the same IC could be connected in parallel, therefore, the total on-resistance of the channel will be kept to a minimum possible value.

During the open or close process, the activation of each relay must be done preventing a short circuit. So, a break-before-make strategy will be implemented. The switching algorithm will include a simple procedure to avoid short-circuit of paths, first all switches are opened and then the correct configuration is set. A secure time must be included to prevent a short circuit and will be set considering the relay specifications. The S3 relay must be closed after the secure time too.

The slave board will have a switch to connect the guard/ground of the connected device to the multiplexer ground.

The slave board will include connectors for analog signals, supplies, and control signals. The following table shows these requirements.

**Table 1:** slave board connectors.

|  |  |  |
| --- | --- | --- |
| **Identification** | **Uses** | **Connector** |
| Control | 3.3 V digital signal | Ribbon Cable.  PMOD type |
| Supply | Voltage supply  Two connectors in parallel to connect the boards in cascade. | Molex type connectors |
| Way 1, Way 2, Pole | Analog signals | Isolated BNC, SMA, SMB or Binding Post  SMA preferred for internal interconnections |
| Binding post | Guard | Binding Post |

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### Additional description

* Isolated digital signals (galvanic isolator delay 20 ns ISO7340)
  + 1 digital line per channel to activate signals relay
  + 1 digital line per channel to activate ground relay
  + 1 digital line per channel to activate ground way relay
  + 1 digital line per channel to activate ground pole relay
  + In total 4 lines per channel
* Protection
  + Overvoltage protection by transient suppression diodes
  + Overcurrent protection by series relay controlled by current measurement
  + The protection will be includes at pole and ways (reversible design)

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## Master board

The master board is a commercial FPGA board, its functionalities are:

1. Control the slave board states. The master board must include at least four channels to control four slave boards.
2. The FPGA can generate an output clock based on its internal clock or an external signal.
3. The master 0board will be configured and set by USB port, the following actions will be possible:
   * save a switching sequence
   * to configure a single channel
   * to configure out clock
   * to configure source clock

The master board will include timing and control connectors as is shown in the following table.

**Table 2:** Master board connectors

|  |  |  |
| --- | --- | --- |
| **Identification** | **Functionality** | **Connector** |
| Slave connectors | Digital signal and supply to slave units | Ribbon Cable.  PMOD type |
| Supply | Supply from main power adapter | Molex connector |
| Clock IN | 10 MHz signal (opto-isolated) | Isolated BNC, SMA, SMB or Binding Post  SMA preferred for internal interconnections |
| Clock OUT | Output clock based on clock IN | Isolated BNC, SMA, SMB or Binding Post  SMA preferred for internal interconnections |
| Trigger | To trigger the sequence or/and the switching (opto-isolated) | Isolated BNC, SMA, SMB or Binding Post  SMA preferred for internal interconnections |
| USB | To connect to PC | USB |

### Switching sequence

The switching sequence is transferred to the FPGA by USB port and internally stored for further uses. The switching sequence can be considered as a matrix where each row represents the state of all the slave boards. The transition between each row will be controlled by a switching event. The user can configure the row value and in practice no more than 1024 rows will be necessary. For example, if 4 slave boards are connected in a 4 step process:

**Table 3:** Switching sequence matrix.

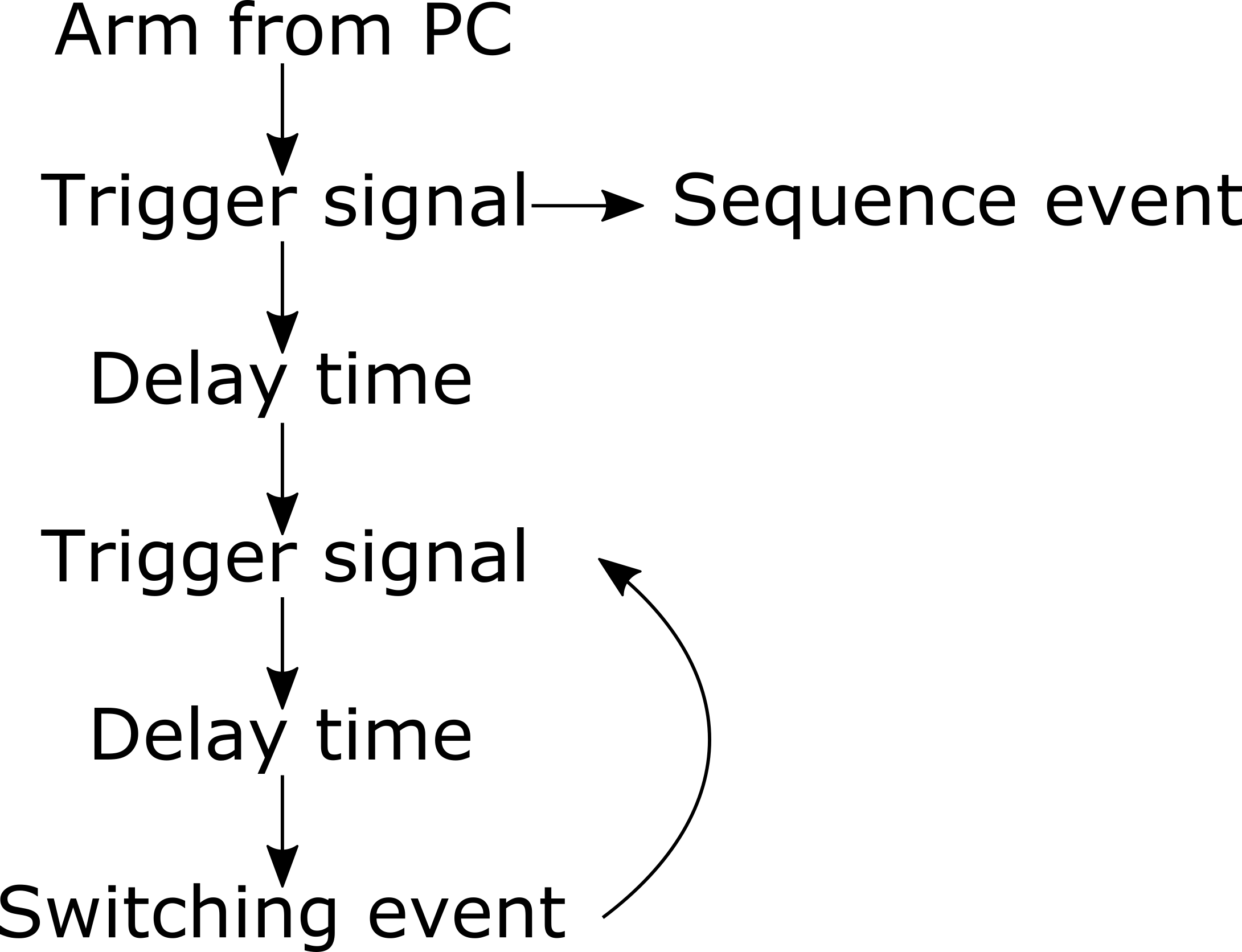
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Step | Slave 1 | Slave 2 | Slave 3 | Slave 4 | Delay time (number of internal or external clock) |
| 1 | Off | On | Off | Off | 10 |
| 2 | On | Off | Off | Off | 15 |
| 3 | Off | Off | On | Off | 15 |
| 4 | Off | Off | Off | On | 10 |

**Se especifica canal 1, canal 2 o abierto.**

A trigger tree is considered to control the switching sequence, first the master board is armed and then a sequence starts with a sequence event. A switching event determines a multiplexer switch.

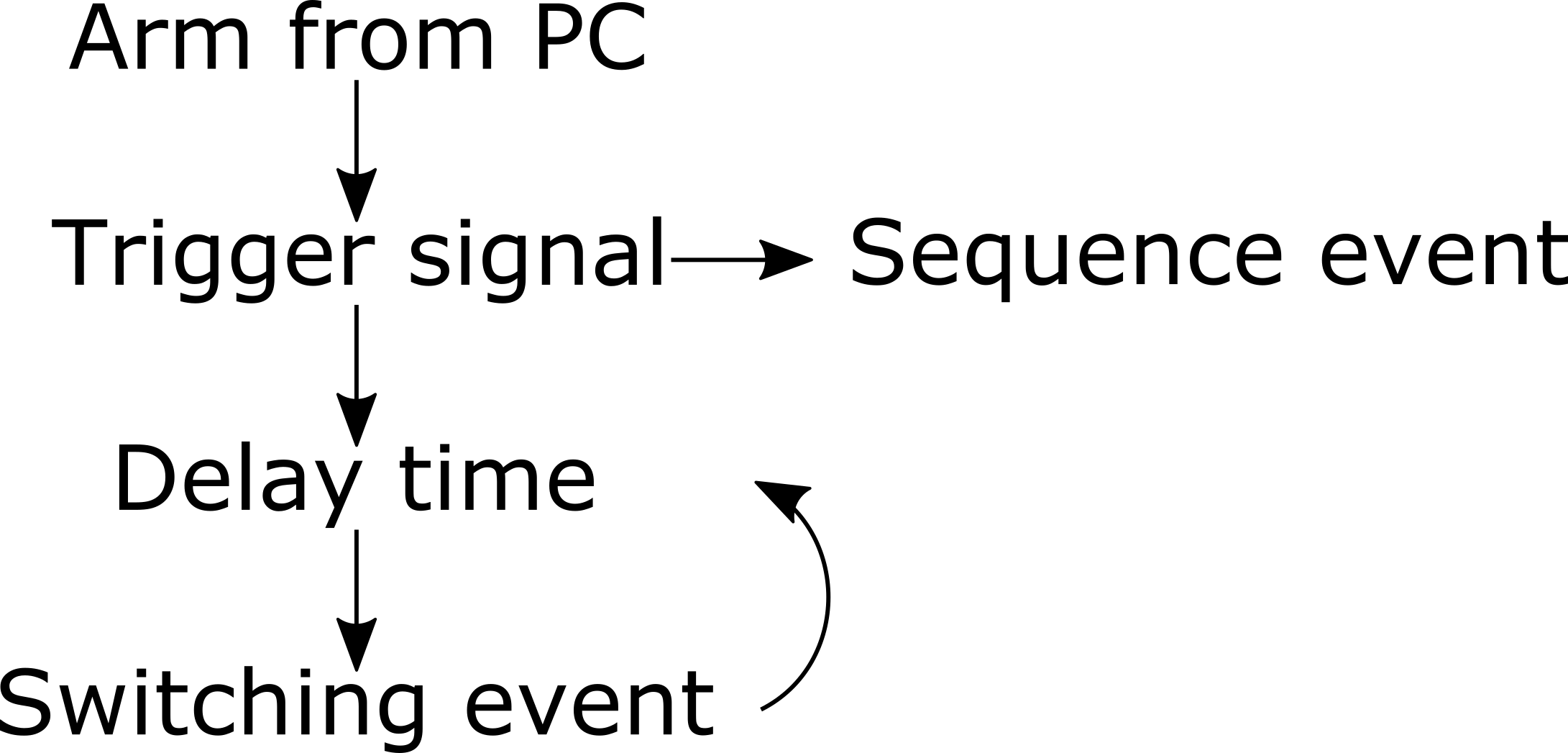
The arm message is provided by the PC and the disarm message, also from PC, ends the switching sequence. The scanner will remain armed until a sequence event is produced, this event is defined as a trigger signal at trigger BNC. Then the scanner switches between channels synchronized with a switching event. The mode of the switching event can be external or Internal.

* External: the switching of all the slave boards is commanded by an external trigger signal in the corresponding trigger BNC connector. This same signal defines the sequence event after the arm message. The switching event is generated if the external signal is ON and after a delay time, which is based on the internal FPGA oscillator or an external clock. The following figure presents a possible trigger tree.



**Figure 4:** trigger tree for external trigger.

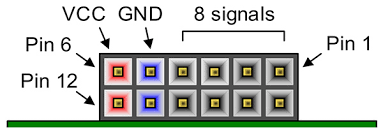
* Internal: the switching event is produced after a delay time from the last switching. That time is based on the internal FPGA oscillator or an external clock.



**Figure 5:** trigger tree for internal trigger.

### FPGA requirement

* Clock speed faster than or equal to 100 MHz.
* More than 40 IO pins (pins for slave board: 4, 1 for clock out, 1 for in clock, 1 for trigger)
* Off-the-shelf / Easy to buy / Open source compatible
* At least USB/UART communication
* Standard connector (PMOD - Arduino - Raspberry)
* Hardware description load by SD card



**Figure 6:** PMOD connector used in many FPGA development kits.

### FPGA Hardware description

The FPGA can be considered as a state machine with just two states, the Switching state and the Configuration state. The transitions between them is produced by a command from PC:



**Figure 7:** state machine with just two states.

### Switching state pseudo-algorithm

1. The switches that connect the source ground are activated, they are not modified during the sequence.
2. The FPGA detects a Sequence event.
3. Switching procedure
   1. All the switches are opened.
   2. A secure time is waited in order to prevent a short circuit. The secure time is 2 times the specification of the relay.
   3. The correct sequence is configured. The sequence will be saved in a matrix, so the FPGA can take the configuration from each row. The GND switches of the OFF channels are activated to improve OFF-Isolation.



**Figure 8:** time diagram of the switching.

1. A counter to indicate the following matrix row is incremented.
2. The FPGA waits for a switching event and returns to point 3.
   1. In external mode the switching event is obtained after a trigger signal and a delay time.
   2. In internal mode the switching event is obtained after a delay time.
3. If a disarm command is received the FPGA returns to turn-on state.

### Configuration state pseudo-algorithm

1- The FPGA detects slave boards connected **(Esto lo vamos a tener que sacar porque no tenemos suficientes señales lógicas)**

2- Al encender o reset el multiplexer se tiene que estar en el siguiente estado:

-Todos los canales abiertos (CH1\_ENA = CH2\_ENA = FALSE)

-Todas las guardas desconectadas (abiertas) (CH1\_GND = CH2\_GND = FALSE)

-Todos los canales con GND cerrada. (CH1\_GRD = CH2\_GRD = TRUE)

3- The FPGA gives the information of slaves boards to the PC **(Esto lo vamos a tener que sacar porque no tenemos suficientes señales lógicas)**

4- The FPGA waits for the

Sequence

trigger configuration

Internal or external trigger

Frequency divider

Hardware-parameters

5- When the multiplexer is armed from the PC, the FPGA goes to the Switching state.

### Error check detection

* Just one channel per slave can be activated at the time (esto se podría modificar si se usan dos digitalizadores)
* The GND relay and Channel relay can not be activated at the same time

### Trigger and out clock generator

Input clock 10 MHz or 20 MHz

The output clock is a submultiple of the input clock.

The frequency divider is a configuration.